REMARKS/ARGUMENTS

Claims 9-11 stand rejected under 35 U.S.C. 102(b) as being anticipated by Tran; claims 5-7 and 13-15 stand rejected under 35 U.S.C. 102(a) as anticipated by, or, in the alternative, under 35 U.S.C. 103(a) as obvious over, Han.

In rejecting claim 9 the examiner states, in the action dated 1/26/2004, that the pass gate (76) of the circuit shown in the Tran et al. patent is a pulling down the voltage B. This statement does not reflect the operation of the circuit shown in the Tran et al. patent. As described in the Tran et al. patent, the pull down network comprises circuit element 74. This circuit element is connected to VSS and functions to pull the voltage of point A (and point B) to VSS. The function of the pass element 76 is differentiated from the pull down element as follows:

When the element 74 is switched on, the voltage at point A will necessarily be pulled down to VSS. However when either transistor in the element 76 is switched on the voltage at point b will not necessarily be pulled down to VSS. In other words the element 76 does not function to pull the voltage at point B down to VSS. The pull down is determined by whether the element 74 is switched on. The element 76 functions only to pass the voltage at point A to point B and vice versa. Therefore the function of element 76 is as a pass transistor circuit as clearly spelled out in the Tran et al. patent. The examiner is incorrect in the description of the Tran et al. patent and claim 9 is allowable over the cited art. Claims 10 and 11 depend on claim 9 and contain all the limitations of claim 9. Claims 10 and 11 are therefore also allowable over the cited art.

In rejecting claims 5-7 and 13-15 the examiner states that the Han et al patent describes a, "pull-down network (422-2) comprising a plurality of series (not shown but inherent that when NAND/AND function is desired for the PMOS logic block; for example, see 27 in Fig. 2 of Gupta et al. for series connection of transistors) connected PMOS transistors." This statement does not comport with the current understanding and interpretation of the meaning of inherency. The reference describes the blocks 412-1,

412-2, 422-1, and 422-2 as NMOS and PMOS logic blocks respectively. It is not inherent in a "logic block" just what the internal connections of the transistors are since the "logic block" encompasses all possibilities. Furthermore the example the examiner cites to support the claim of inherency (27 in Fig. 2 of Gupta et al.) shows all NMOS transistors connected in series and not the PMOS transistors claimed in claims 5 and 13. Clearly there is no inherency in the Han et al. patent. Furthermore, the examiners own example cited to support the claim of inherency shows NMOS transistors and not PMOS transistors. Finally, the examiner argues that the selection of series connected PMOS transistors is an obvious matter of design choice. This type of hindsight analysis is not allowed under current U.S.C. 103(a) and claims 5 and 13 are allowable over the cited art. Claims 6 and 7 depend on claim 5 and contain all the limitations of claim 5. Claims 6 and 7 are therefore also allowable over the cited art. Furthermore, claims 14 and 15 depend on claim 13 and are also allowable over the cited art.

Applicant appreciates the indication that claims 1-4, 8, 12, and 16 are allowable.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including

extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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